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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/871,596

05/30/2001

Noriyuki Saruhashi

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26021

7590

10/19/2004

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EXAMINER

TORRES, JOSEPH D


ART UNIT

PAPER NUMBER

2133

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/871,596	Applicant(s) SARUHASHI ET AL. 	
	Examiner Joseph D. Torres	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 September 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 May 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

1. In view of the Amendment filed 30 July 2004, all objections to the claims are withdrawn.

Claim Rejections - 35 USC § 112

2. In view of the Amendment filed 30 July 2004, all previous 35 USC § 112 rejections to the claims are withdrawn.

Response to Arguments

3. Applicant's arguments filed 27 September 2004 have been fully considered but they are not persuasive.

The Applicant contends, "the cited reference does not teach nor suggest the limitation of said first port is connected to a second port that is one of said plurality of ports through an external bus, and the second port is connected to said physical layer logic circuit as described in the claims of the present invention". More specifically, claim 1 recites, "a plurality of ports to be connected to said physical layer logic circuit are provided beforehand in said physical layer device; in testing, test link layer circuit is connected to said physical layer logic circuit through said link layer interface, and test physical layer logic circuit is connected to a first port that is one of said plurality of ports, and said first

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port is connected to a second port that is one of said plurality of ports through an external bus, and the second port is connected to said physical layer logic circuit".

The Examiner asserts that Shinozuka teaches test circuitry 40 of Figure 1 of Shinozuka to be incorporated into the Serial Bus Experimental Apparatus 2_n of Figure 6.

Shinozuka teaches a plurality of ports, 1₁, 1₂,...1_{n-1} in Figure 6 of Shinozuka to be connected to physical layer logic circuit 4_n are provided beforehand in physical layer device Serial Bus Experimental Apparatus 2_n; in testing, test link layer circuit Controller 3_n (col. 2, lines 19-23 in Shinozuka teaches Controller 3_n is used for bus testing at the link layer during bus testing, hence Controller 3_n is a test link layer circuit) is connected to physical layer logic circuit 4_n through said link layer interface 5_n, and test physical layer logic circuit 40 in Figure 1 of Shinozuka is connected to a first port 1_{n-1} (via physical layer logic circuit 4_n) that is one of said plurality of ports 1₁, 1₂,...1_{n-1}, and said first port 1_{n-1} is connected to a second port 1_{n-2} that is one of said plurality of ports 1₁, 1₂,...1_{n-1} through an external high performance serial bus 1 in Figure 6 of Shinozuka, and the second port 1_{n-2} is connected to said physical layer logic circuit 4_n via said first port 1_{n-1}.

The Examiner disagrees with the applicant and maintains all rejections of amended claims 1-3. All amendments and arguments by the applicant have been considered. It is the Examiner's conclusion that amended claims 1-3 are not patentably distinct or non-obvious over the prior art of record in view of the reference, Shinozuka, Satoshi (US

6560200 B1) as applied in the last office action, Paper No. 9 (filed 03 March 2004).

Therefore, the rejection is maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Shinozuka, Satoshi (US 6560200 B1).

See Paper No. 9 (filed 03 March 2004) for detailed action of prior rejections.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

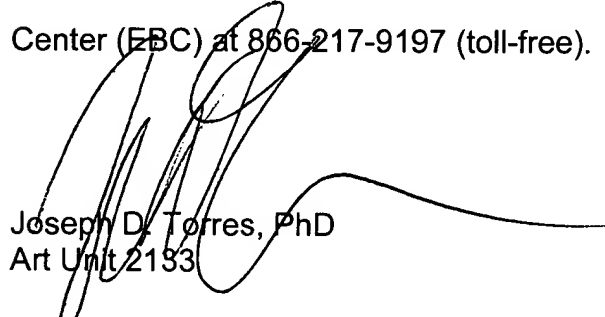
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extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Joseph D. Torres, PhD
Art Unit 2133


Guy J. LAMARRE
PRIMARY EXAMINER